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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,445	FURUSHO, SHINJI	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-28,30,31,33,36-38,40,41,43 and 45-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-28,30,31, 33,36-38,40,41, 43 and 45-50* is/are rejected.

7)☒ Claim(s) *33 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 8/27/2008. At this point claims 26-28, 30, 31, 33, 36-38, 40, 41, 43, and 45-50 have been amended and claims 29, 32, 34, 35, 39, 42 and 44 have been cancelled. Thus, claims 26-28, 30, 31, 33, 36-38, 40, 41, 43, and 45-50 are pending in the instant application.

The instant application having Application No. 10/553,445 has a total of 18 claims pending in the application, there are 5 independent claims and 13 dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

As required by **M.P.E.P. ' 609 (C)**, the applicant's submission of the Information Disclosure Statement, dated 7/10/2006, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P. ' 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

The information disclosure statement fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language (CN 1,423,772). While it is listed in the preliminary report on patentability, it is unclear

what the relevancy of that particular document is. It has been placed in the application file, but the information referred to therein has not been considered.

CLAIM OBJECTIONS

Claim 27 and its dependent claims are objected to because of the following informalities: "item value numbers indicting"; the phrase has been construed "item value numbers indicating". Appropriate correction is required.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-28, 30, 31, 36-38, 40, 41, and 45-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furusho '332 (EP 1,233,332) in view of Furusho '918 (EP 1,136,918)

Regarding Claim 26, Furusho '332 teaches an information processing system comprising:

(a) a plurality of information processing units arranged in a ring shape, (Blocks 14-1 to 14-4 in Figure 1, also, each processor is connected to each other, which may be represented logically as a ring shape) each unit holding a local information block (such

as the blocks in Figure 6) to represent tabular data expressed as an array of records including item values belonging to respective items (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries, such as 'Carter'); and

(b) a packet transmission path to connect the plurality of information processing units (bus 26 in Figure 1, described in paragraph 0034); and

each of the information processing units include:

i. means for creating, based on the local sequence numbers in the local information block (this local order is indicated by the 'subscripts' as described in paragraph 0052), unique global sequence numbers in all of the plurality of information processing units (all elements are ordered during the merge in step 710 in Figure 7, also see paragraph 0086, also see Column 2 Line 55 to Column 3 Line 21, where it is made clear that the information on the individual processor modules are first ordered before a global order [the global order indicated by virtual sequence numbers, Column 19 Lines 22-26] is decided);

ii. means for transmitting the value list to one adjacent information processing unit through the packet transmission path (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another processor, thus the processors are able to give and receive value lists);

iii. means for receiving the value list from an other second adjacent information processing unit through the packet transmission path (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another

processor, thus the processors are able to give and receive value lists); and

iv. means for giving a global sequence number across all the plurality of information processing units to the item value in the value list in the local information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from previous processors, see paragraphs 0058 and 0060), wherein a duplicate item value in the item values in the value list from the other second information processing unit is deleted when there is a duplicate value between the value lists transmitted to the first information processing unit and received from the other second information processing unit (the transfer of values in Furusho '332 "are not redundant", and duplicates are gotten rid of, Paragraph 0126);

However, Furusho '332 does not explicitly teach how the records are stored within the processors. Furusho '918 teaches storing information on a local information block, including a value list in which the item values are stored in order of item value numbers indicating positions of the item values in the value list (see Figure 7, where the item value 'age' numbers are stored in order), and a pointer array in which pointer values indicate the item value numbers stored in order of unique local sequence numbers corresponding to the records (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the

records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 27, Furusho '332 teaches an information processing system comprising:

(a) a plurality of memory modules arranged in a ring shape, each having a memory, an interface, and a control device (memory modules 14, which have memory for storing data as shown in Figure 4, an interface as shown Figure 3, and a controller corresponding to a processor as described in Paragraph 0051, also, each processor is connected to each other, which may be represented logically as a ring shape); and

(b) a packet transmission path connecting interfaces of adjacent memory modules (bus 26 in Figure 1, described in paragraph 0034),

and a global information block is formed of an aggregate of the information blocks held in the respective memories (see paragraph 0086, where the sequence of all elements are determined, and from this global array [corresponding to a global information block] can be determined in step 711 of Figure 7),

the control device of each of the memory modules includes:

i. offset value storage means for holding an offset value to indicate which position that the information block held by this memory module occupies in the global information block (this offset is indicated by the 'subscripts' as described in paragraph 0052);

ii. global ordered set array creation means for creating, based on the offset

value, a global ordered set array containing global sequence numbers corresponding to the records in the global information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found based on the offset values [subscripts as defined in paragraph 0052] from previous processors, see paragraphs 0058 and 0060);

iii. packet transmission means for packetizing the value list for each item held by the memory module and transmitting the value list to one adjacent second memory module by using the transmission path (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another processor, thus the processors have packet transmission to transmit value lists);

iv. packet reception means for receiving a packetized value lists held by other third memory modules from an other adjacent fourth memory module by using the transmission path in parallel to packet transmission by the packet transmission means (see beginning of paragraph 0063, where two elements [corresponding to the value list] are transmitted to another processor, thus the processors have packet reception means to receive value lists); and

v. order judgment means for determining a global sequence number of the item value in the value list held by this memory module across the global information block module and for storing the global sequence number of the item value in the value list held by this memory module into a global value number array for each item (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values

[subscripts as defined in paragraph 0052] from previous processors, see paragraphs 0058 and 0060, thus the processors have order judgment means, and once this global order is found it is stored in the global information block as constructed in step 711 of Figure 7), wherein the value list held by this memory module is compared with each of the received value lists, a duplicative value from each of the received value lists, a duplicative value from each of the received value lists is deleted when there is a duplicative value between the value list held by this memory module and each of the received value lists, and the relative sequence number is determined in relation to this value list (the transfer of values in Furusho '332 "are not redundant", and duplicates are gotten rid of, Paragraph 0126).

However, Furusho '332 does not explicitly teach how the records are stored within the memory modules. Furusho '918 teaches where memory of each of the memory modules contain item values which are stored in order of item value numbers corresponding to the item values belonging to a specific item (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category), and a pointer array having pointer values that indicate the item value list and also includes a pointer array having pointer values that indicate the item value numbers stored in order of unique local sequence numbers corresponding to the records (the pointer array corresponding to the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]).

It would have been obvious to a person having ordinary skill in the art to which

the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 28, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and Furusho '332 further teaches wherein the information processing system further comprises record extraction means for specifying a value in the global ordered set array in accordance with an instruction to specify a sequence number of the record (see the extraction of paragraph 0012, where the record number is the value in the global ordered set array and the extraction must be done in accordance with an instruction) and extracting the record indicated by the specified value (the values corresponding to this record are extracted, note how all data field values can be extracted as in the last sentence of paragraph 0012).

Regarding Claim 30, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and the storage table of Furusho '918 further includes:

flag array setup means for creating a flag array with a same size as the value list for an item to be retrieved and for setting a specific value to an element at a position corresponding to an item value satisfying a retrieval condition (see Figure 7, where the value control table is the flag array, since this table is the same size as the value list [one row for each value, or age] and each row contains a specific value [the age] which can be retrieved as in the process of Column 6 Lines 17-23, thus flag array setup

means to create such a table is present);

retrieval condition judgment means for judging, for the item to be retrieved, whether a record corresponding to a value in the ordered set array satisfies the retrieval condition by specifying a value in the pointer array corresponding to a position indicated by the value in the ordered set array (the position corresponding to the entry number of the pointer table in Figure 7) and then by specifying a value in the flag array corresponding to a position indicated by the value in the pointer array (the pointer at the corresponding record specifies the value in the value table of Figure 7, also see Column 6 Lines 8-23, thus such judgment means are present);

and Furusho '332 teaches a local retrieval means for storing the value in the ordered set array satisfying the retrieval condition (see Figure 6, where the set is ordered with the retrieval condition corresponding to the last name) and a corresponding value in the corresponding global ordered set array into a second ordered set array and a second global ordered set array, respectively, (where the re-ordered set of Figure 6 corresponds to the second global ordered set array),

wherein the packet transmission means packetizes and transmits the second global ordered set array to the one adjacent second memory module using the transmission path, the packet reception means receives the packetized second global ordered set arrays from the other adjacent fourth memory module (see beginning of paragraph 0063, where two elements [corresponding to the global ordered list] are transmitted to another processor, thus packet transmission and reception means are present),

the control device of each of the memory modules further includes second order judgment means for determining sequence number of the value the second global ordered set array held by this memory module across the global information block by referring to the received second global ordered set and for storing the determined sequence number across in the global information block into a third global ordered set array (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from the second global ordered set [subscripts as defined in paragraph 0052] from previous processors, see paragraphs 0058 and 0060, thus second order judgment means are present, and once this global order is found it is stored in a third global ordered set array as constructed in step 711 of Figure 7 and explained in paragraph 0086), and

a sequence number of a record satisfying with the retrieval condition is decided by the value of the third global ordered set array (a new ordered array is generated as in Column 26 Liens 23-28).

Regarding Claim 31, Furusho '332 and Furusho '918 teach the information processing system according to claim 27, and Furusho '918 further teaches wherein the control device further includes

contains count-up means for creating counting up values in a logical coordinate array having a size equal to a product of sizes of value lists for items to be tabulated by the number of records held by this memory module for each of sets of item values for the items to be tabulated, wherein the values in the logical coordinate array indicate the

number of sets of global sequence numbers of the item values across the global information block (such a logical coordinate array corresponding to the Table of Figure 26, also see process for creating this table in Figure 20, note how the number of entries [size] is calculated by multiplying the number of item values [3 for gender and 5 for occupation, resulting in 15 values], also see steps 204, 206, 208, and 210 in Figure 22), and

wherein the packet transmission means packetizes and transmits the logical coordinate array, to which count-up has been applied by the count-up means, to one adjacent fifth memory module through the transmission path (see beginning of paragraph 0063 in Furusho '332, where two elements [containing the logical coordinate array of Furusho '918] are transmitted to another processor, thus packet transmission and reception means are used and the array transmitted),

wherein the packet reception means receives the counted up logical coordinate array from the other adjacent fourth memory module through the transmission path path (Paragraph 0086 in Furusho '332, where a global order is given ["sequence number of all elements are determined"], and thus the counts are made again at the time of re-tabulation of the global sequence, note Column 5 Lines 43-49 in Furusho '918, particular where the count-tables become 'usable at the time of tabulating'), and

global numbers of the records for each set of the item values for the respective items are stored in the logical coordinate array by repeating the reception, count-up and transmission of the logical coordinate array among the control devices of the respective memory modules (Paragraph 0086 in Furusho '332, where a global order is given

["sequence number of all elements are determined"], and thus the counts are made again at the time of re-tabulation of the global sequence, note Column 5 Lines 43-49 in Furusho '918, particular where the count-tables become 'usable at the time of tabulating').

Regarding Claim 33, Furusho '332 and Furusho '918 teaches all limitations of claim 27 as described above, and Furusho '918 further teaches the control device of each of the memory modules includes:

existence number array creation means for creating an existence number array with the same size as that of a value list for an item to be sorted and for arranging numbers of values in the existence number array (the logical count-up array corresponding to the 'count' category array of Figure 7, which is the same size as the value array on the other side of the table), the values in the the ordered set array specifying respective item values in the value list (each entry in the array is a count of the number of values in the ordered set array, thus, since such an array is created, existence number array creation means are present) ;

accumulated number array creation means for accumulating the values in the existence number array, calculating accumulated numbers to indicate head positions of records having corresponding item values at a time when the sort is performed in this memory module (the table of Figure 7 contains a start [head] position of the records having the corresponding item value at that particular row position, and since this array is created at the time of tabulating as described at the end of paragraph 0017, the item value of the record corresponds to when the sort was performed), and arranging the

accumulated numbers in an accumulated number array (the accumulated number is clearly arranged in the array as shown in Figure 7); and Furusho '332 further teaches

local sort means for creating a second global value number array, a fourth global ordered set array and a third ordered set array (each memory unit 14 has a local sort means that re-sorts the data [as shown in Figure 6] and forms second, third, and fourth set arrays which contain global sequence numbers, see paragraphs 0054 and 0055 in Furusho '332), and arranging a global value number corresponding to the item value in the second global value number array, (Paragraph 0086, where a global order is given based on an item value ["sequence number of all elements are determined"]), the value of the ordered set array in the third ordered set array and the value of the corresponding global ordered set array in the fourth global ordered set array at respective positions indicated by the accumulated number based on the accumulated number in the accumulated number array corresponding to the item value indicated by the value of the ordered set array (note how the process applied to the first and second arrays is done in a similar fashion to the third and fourth arrays, see Paragraph 0069 in Furusho '334, also, this global order is found by referring to item values from the second global ordered set from previous processors as shown in Paragraphs 0058 and 0060, and since a sequence is given according to these item values as described in Paragraph 0060, and the set array stores the beginning of the sequences of the item values, that this order is found by referring to the position of the accumulated number);

wherein the packet transmission means packetizes and transmits at least the second global value number array to the one adjacent second memory module through

the transmission path, while the packet reception means receives a packetized second global value array from the other fourth adjacent memory module through the transmission path in parallel to the second global value number array being transmitted to the one adjacent second memory module (see beginning of paragraph 0063 in Furusho '332, where two elements [containing the array of Furusho '918] are transmitted to another processor, thus packet transmission and reception means are used and the array transmitted), and

the control device of each of the memory modules further includes third order judgment means for storing a sequence number of a value in the second global value number array held by this memory module into a fifth global ordered set array by referencing to the received second global value number arrays, wherein the sequence number of the value is determined in the global information block (a new fifth order set array is created as in Paragraph 0086, and this is of course based on the value of the ordered global information blocks because of the processing done in paragraphs 0058 and 0060), and

a sequence number of the sorted record is defined by the value contained in the fifth global ordered set array (since the fifth global order is stored as in paragraph 0086, the order of the sorted records is decided by it).

Claim 36 is the method equivalent of Claim 26 and is rejected under similar rationale.

Claim 37 is the method equivalent of Claim 27 and is rejected under similar rationale.

Claim 38 is the method equivalent of Claim 28 and is rejected under similar rationale.

Claim 40 is the method equivalent of Claim 30 and is rejected under similar rationale.

Claim 41 is the method equivalent of Claim 31 and is rejected under similar rationale.

Claim 43 is the method equivalent of Claim 33 and is rejected under similar rationale.

Claim 45 is the program equivalent of Claim 26 and is rejected under similar rationale.

Regarding Claim 46, Furusho '332 teaches an information processing system comprising:

a plurality of information processing units arranged in a ring shape, each unit including a memory and a control device (memory modules 14, which have memory for storing data as shown in Figure 4, an interface as shown Figure 3, and a controller corresponding to a processor as described in Paragraph 0051 also, each processor in Figure 1 is connected to each other processor, which may be represented logically as a ring shape),

wherein the memory holds tabular data expressed as an array of records each including item values belonging to respective items, (where the items correspond to the entries in Figure 6 and the item values correspond to the values contained in these entries, such as 'Carter'), and

global tabular data is formed of an aggregate of the tabular data held by the information processing units (as in paragraph 0086), wherein

the global tabular data contains, for each item, unique global sequence numbers of the item values held by all of the information processing units, the unique global sequence numbers (all elements are ordered during the merge in step 710 in Figure 7, also see paragraph 0086, also see Column 2 Line 55 to Column 3 Line 21, where it is made clear that the information on the individual processor modules are first ordered before a global order [the global order indicated by virtual sequence numbers, Column 19 Lines 22-26] is decided) are given to the item values by deleting a duplicate item value (the transfer of values in Furusho '332 "are not redundant", and duplicates are gotten rid of, Paragraph 0126),

and each of the information processing units includes:

a global ordered set array containing values indicating sequence numbers of records in the global tabular data (all elements are ordered during the merge in step 710 in Figure 7, also Figure 12, where the global sequence is shown to be formed).

However, Furusho '332 does not explicitly teach record extraction means. Furusho '918 teaches

record extraction means for identifying a value in the global ordered set array in accordance with an instruction to specify a sequence number received by the control device of the respective information processing unit (see the extraction of paragraph 0012, where the record number is the value in the global ordered set array and the extraction must be done in accordance with an instruction), and for extracting the record

indicated by the identified value in the global ordered set array (the values corresponding to this record are extracted, note how all data field values can be extracted as in the last sentence of paragraph 0012).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

Regarding Claim 47, Furusho '332 and Furusho '918 teach all limitations of Claim 46 as described above. Further, Furusho '332 teaches the information processing unit holds a further ordered set array in which the values identifying the records are permutated

in order to reflect a sort order in the respective information processing unit, (in the case where the data is exchanged among the processing units as in Column 22 Lines 11-16) ,

and rearranges the values indicating the sequence numbers in the global ordered set array in order to reflect a sort of order of the record in the global tabular data, wherein the record is specified by the value in the further ordered array (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19).

Regarding Claim 48, Furusho '332 and Furusho '918 teach all limitations of Claim 46 as described above. Further, Furusho '332 teaches the information

processing unit to be characterized in that the information processing unit rearranges the values indicating the sequence numbers, in the global ordered set array, of the record in the global tabular data, wherein the record is sorted in the respective information processing unit (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19).

Regarding Claim 49, Furusho '332 and Furusho '918 teach all limitations of Claim 46 as described above, and Furusho '918 further teaches characterized in that the information processing unit rearranges the value indicating the order to indicate the so (note the global sequence values indicating the order is rearranged because of this exchange in Figures 16-19) that a memory of each of the information processing units holds an information block (the memory information block corresponding to the blocks as in Figure 10 in Furusho '332) arranged to represent tabular data expressed as an array of records including item values belonging to respective items, the information block including a value list having the item values stored in order of item value numbers indicating positions of the item values in the value list (see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category) and

and a pointer array in which pointer values to indicate the item value numbers are stored in order of unique local sequence numbers corresponding to the records (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]), and

a global information block is formed of an aggregate of the information blocks

held by the respective memories (as in Paragraph 0086 in Furusho '332).

Regarding Claim 50, Furusho '332 and Furusho '918 teach an information processing system comprising

a plurality of information units arranged in a ring shape, each unit including a memory and a control device (memory modules 14, which have memory for storing data as shown in Figure 4 and a controller corresponding to a processor as described in Paragraph 0051, also, each processor is connected to each other, which may be represented logically as a ring shape),

a global information block is formed of an aggregate of the information blocks held by the respective memories (Paragraph 0086, where a global order corresponding to a global information block is given ["sequence number of all elements are determined"], also note that this global order is found by referring to item values from previous processors, see paragraphs 0058 and 0060), and the information processing system is characterized in that the information processing unit includes:

a global value number array to contain a value indicating a sequence number of the item value in the global information block (Paragraph 0086, where a global order is given ["sequence number of all elements are determined"]); and Furusho '918 teaches a table wherein:

a memory of each of the information processing units holds an information block arranged to represent tabular data (the information block as shown in Figure 6) expressed as an array of records each including item values in the value list (where the items correspond to the entries in Figure 6 and the item values correspond to the values

contained in these entries, such as 'Carter', also see Figure 7, where the item value 'age' numbers are stored in order, and the specific item is the 'age' category),

and a pointer array in which pointer values to indicate the item value numbers are stored in order of unique local sequence numbers corresponding to the records, (where the table of pointers on Figure 7 are indexed to a unique local order [since the rows indicate the record number as in the last sentence of paragraph 0012], and they each contain a pointer to the item value [age]), and

item value extraction means for identifying a value in the global value number array in accordance with an instruction to specify sequence number received by the control device of this information processing unit and extracting the item value in the value list indicated by the identified value in the global value number array (see the extraction of paragraph 0012, where the record number is the value in the global ordered set array and the extraction must be done in accordance with an instruction).

It would have been obvious to a person having ordinary skill in the art to which the subject matter pertains at the time the invention was made to have stored the records of Furusho '332 as in Furusho '918, since storing the records this way helps to increase greatly the speed of searching for and tabulating large amounts of data (Paragraph 0009 in Furusho '918).

ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS

Rejections - USC 112

Applicant's arguments/amendments with respect to claims 33-34, 43-44, and 35 have been considered and have overcome the Examiner's prior rejections and thus are withdrawn.

Rejections - USC 101

Applicant's arguments/amendments with respect to claim 45 have been considered and have overcome the Examiner's prior rejection and thus are withdrawn.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's argument with respect to claims 26, 36, 45, and 46 that the modules were not arranged in a ring shape has been considered but is not persuasive. The claim states the processing units are "arranged in a ring shape" but Furusho '332 teaches that all the processors are connected, which may be shown logically as a ring. The exact nature of how the processors are connected to each other is not claimed.

Applicant's argument with respect to claims 26, 27, 36, 37, 45, and 46 that Furusho '332 does not teach deleting duplication data has been considered but is not persuasive. In an embodiment, Furusho teaches erasing pointers of duplicate values in Paragraph 0126, effectively deleting the duplicate values.

CLOSING COMMENTS

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

CLAIMS NO LONGER IN THE APPLICATION

Claims 29, 32, 34, 35, 39, 42, and 44 were cancelled by the amendment dated 8/27/2008.

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 26-28, 30, 31, 33, 36-38, 40, 41, 43, and 45-50 have received a second action on the merits and are subject of a second action final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

December 17, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185